intel®

2117 FAMILY
16,384 x 1 BIT DYNAMIC RAM

	2117-2	2117-3	2117-4
Maximum Access Time (ns)	150	200	250
Read, Write Cycle (ns)	320	375	410
Read-Modify-Write Cycle (ns)	330	375	475

RAM

- **Industry Standard 16-Pin Configuration**
- **±10% Tolerance on All Power Supplies: +12V, +5V, -5V**
- **Low Power: 462mW Max. Operating, 20mW Max. Standby**
- **Low I_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2117 is a 16,384 word by 1-bit Dynamic MOS RAM fabricated with Intel's standard two layer polysilicon NMOS technology — a production proven process for high performance, high reliability, and high storage density.

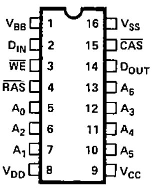
The 2117 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients and ±10% tolerance on all power supplies contribute to the high noise immunity of the 2117 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the 2117 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the 2117 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

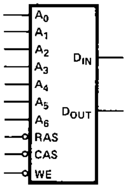
The 2117 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2117 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

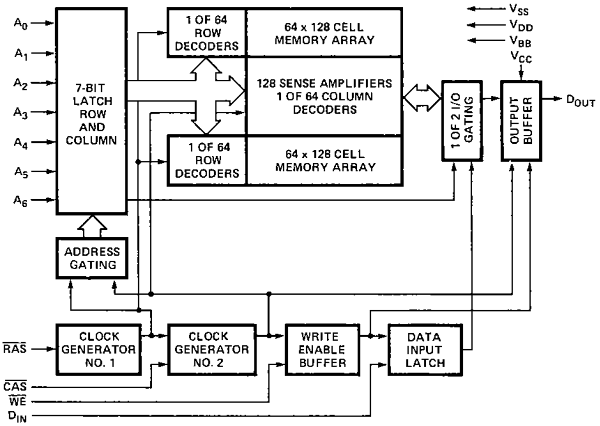
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... -10°C to +80°C
Storage Temperature .... -65°C to +150°C
Voltage on Any Pin Relative to V_{BB}
(V_{SS} - $V_{BB} \geq 4V$) .... -0.3V to +20V
Data Out Current 50mA
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1,2]

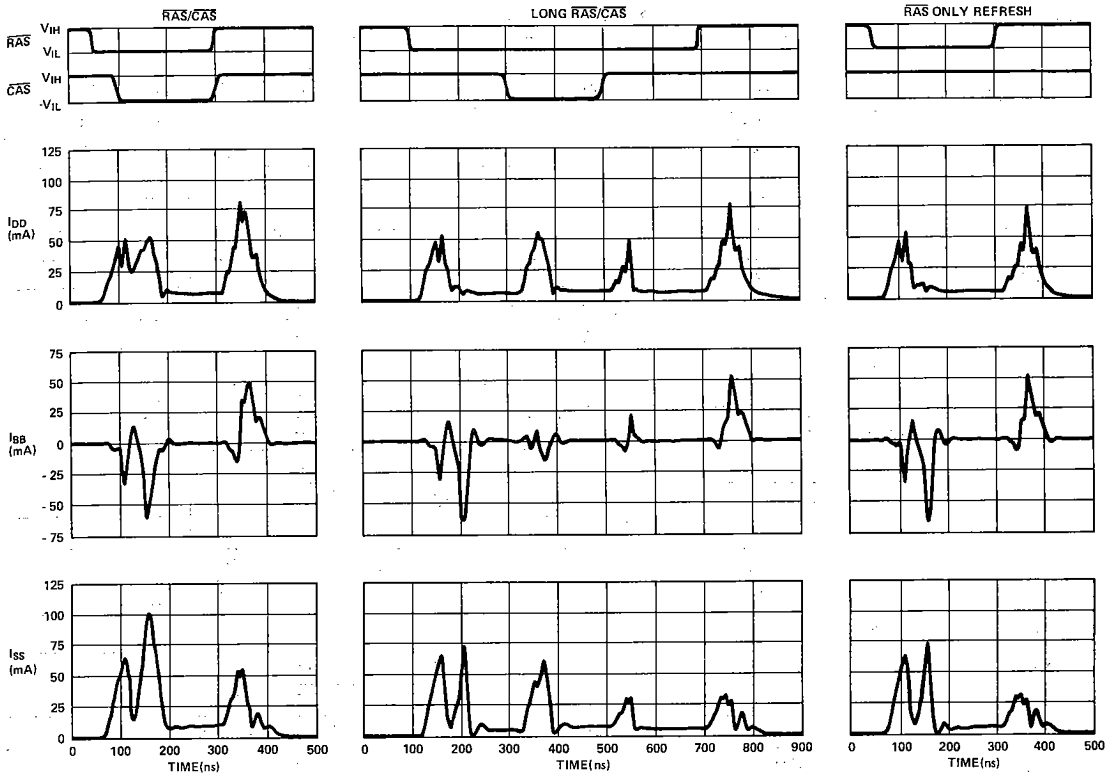
T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Limits Typ.[3]	Limits Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to 7.0V, V_{BB}=-5.0V	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby			1.5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	4
I_{BB1}	V_{BB} Supply Current, Standby		1.0	50	µA		
I_{CC1}	V_{CC} Supply Current, Output Deselected		0.1	10	µA	$\overline{CAS}$ at V_{IH}	5
I_{DD2}	V_{DD} Supply Current, Operating			35	mA	2117-2, t_{RC} = 375ns, t_{RAS} = 150ns	4,6
				35	mA	2117-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				33	mA	2117-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{BB2}	V_{BB} Supply Current, Operating, $\overline{RAS}$-Only Refresh, Page Mode		150	300	µA	T_A = 0°C	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			27	mA	2117-2, t_{RC} = 375ns, t_{RAS} = 150ns	4,6
				27	mA	2117-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				26	mA	2117-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	3	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		6.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	4
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	4

NOTES:
1. All voltages referenced to V_{SS}.
2. No power supply sequencing is required. However, V_{DD}, V_{CC} and V_{SS} should never be more negative than -0.3V with respect to V_{BB} as required by the absolute maximum ratings.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. See the Typical Characteristics Section for values of this parameter under alternate conditions.
5. I_{CC} is dependent on output loading when the device output is selected. V_{CC} is connected to the output buffer only. V_{CC} may be reduced to V_{SS} without affecting refresh operation or maintenance of internal device data.
6. For the 2117-2 at t_{RC} = 320ns, t_{RAS} = 150ns, I_{DD2} max. is 45mA and I_{DD3} max. is 31mA.

RAM

TYPICAL SUPPLY CURRENT WAVEFORMS



Typical power supply current waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (Long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} and I_{BB} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies. Decoupling recommendations are provided in the Applications section.

The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 12.0V$ and $T_A = 25°C$ for two given t_{RAS} pulse widths. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A can be determined by combining the effects of the appropriate family of curves.

CAPACITANCE [1]

$T_A = 25°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$ Capacitance, $\overline{WE}$ Capacitance	4	7	pF
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF
C_O	Data Output Capacitance	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2117-2		2117-3		2117-4		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RAC}	Access Time From $\overline{\text{RAS}}$		150		200		250	ns	4,5
t_{CAC}	Access Time From $\overline{\text{CAS}}$		100		135		165	ns	4,5,6
t_{REF}	Time Between Refresh		2		2		2	ms	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	100		120		150		ns	
t_{CPN}	$\overline{\text{CAS}}$ Precharge Time (non-page cycles)	25		25		25		ns	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	-20		-20		-20		ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	50	25	65	35	85	ns	7
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	150		200		250		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	-10		-10		-10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time, to $\overline{\text{RAS}}$	95		120		160		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	50	0	60	0	70	ns	

READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	320		375		410		ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	150	10000	200	10000	250	10000	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	100	10000	135	10000	165	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	

WRITE CYCLE

t_{RC}	Random Write Cycle Time	320		375		410		ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	150	10000	200	10000	250	10000	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	100	10000	135	10000	165	10000	ns	
t_{WCS}	Write Command Set-Up Time	-20		-20		-20		ns	9
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time, to $\overline{\text{RAS}}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	Data-In Hold Time	45		55		75		ns	
t_{DHR}	Data-In Hold Time, to $\overline{\text{RAS}}$	95		120		160		ns	

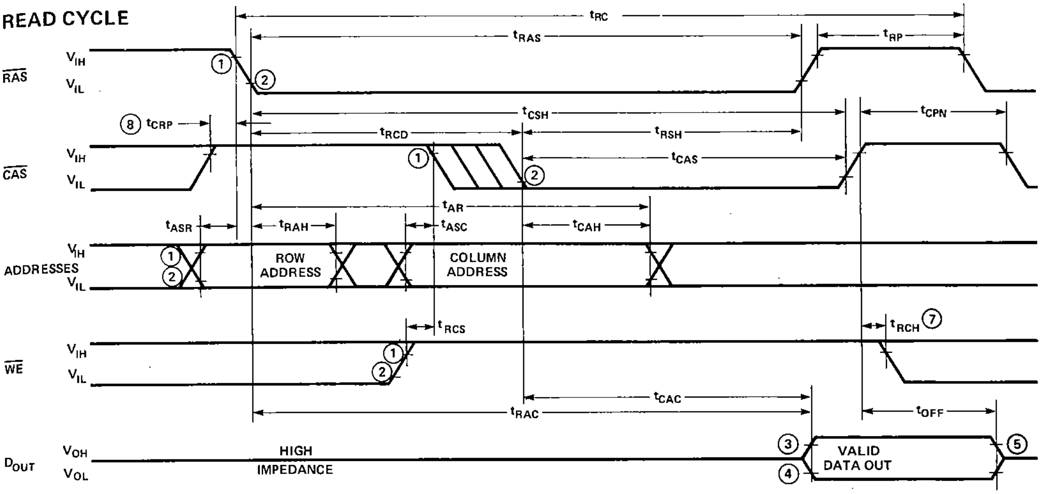
READ-MODIFY-WRITE CYCLE

t_{RWC}	Read-Modify-Write Cycle Time	330		375		475		ns	
t_{RRW}	RMW Cycle $\overline{\text{RAS}}$ Pulse Width	185	10000	245	10000	305	10000	ns	
t_{CRW}	RMW Cycle $\overline{\text{CAS}}$ Pulse Width	135	10000	180	10000	230	10000	ns	
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	120		160		200		ns	9
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	70		95		125		ns	9

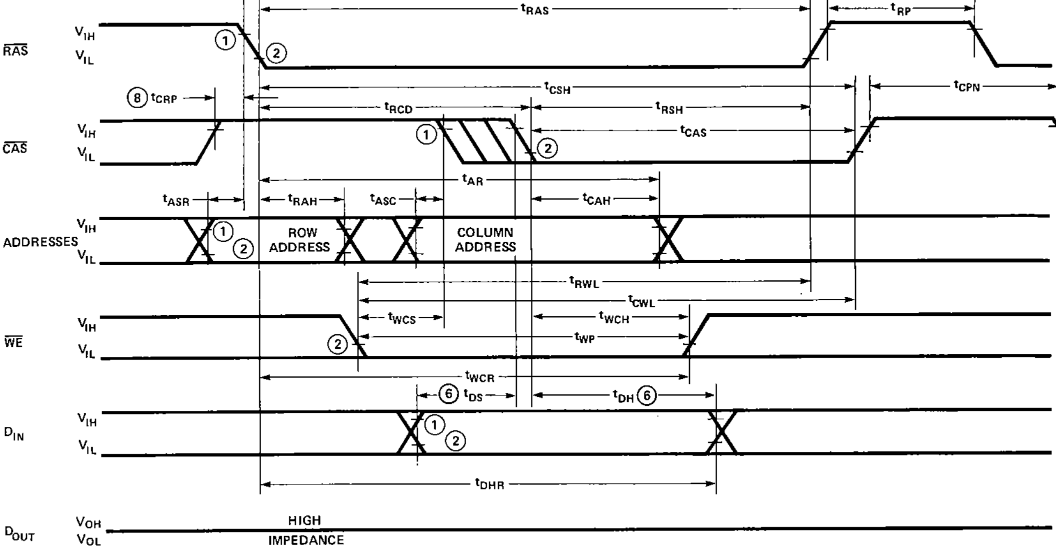
Notes: See following page for A.C. Characteristics Notes.

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}/\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

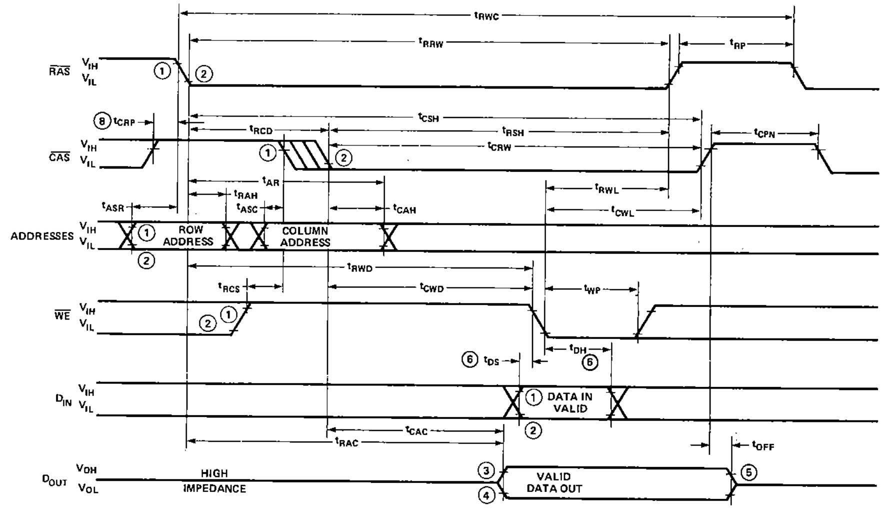
A.C. CHARACTERISTICS NOTES (From Previous Page)

1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume $t_T = 5ns$.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}, if t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

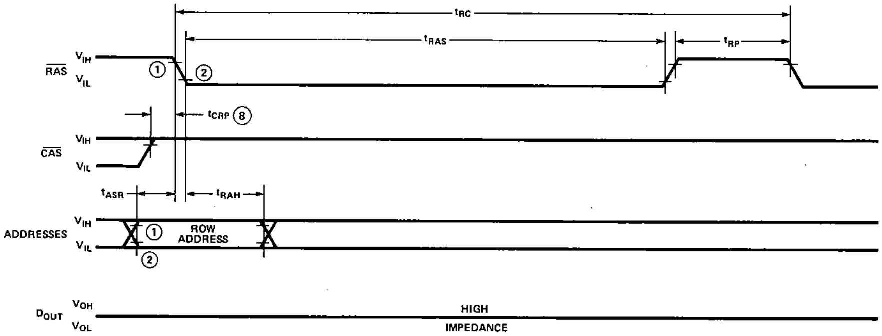
RAM

WAVEFORMS

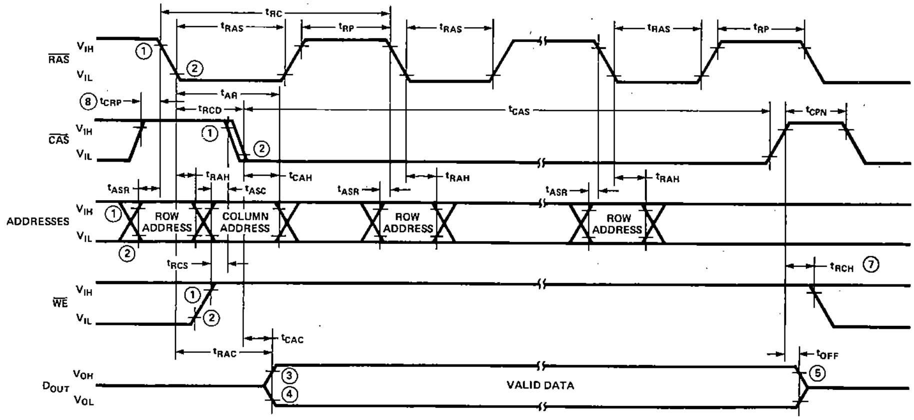
READ-MODIFY-WRITE CYCLE



$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



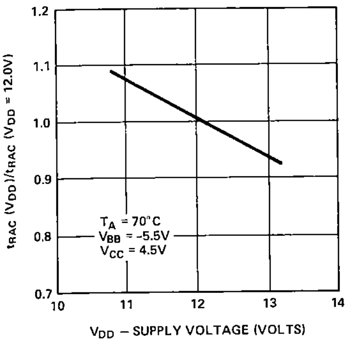
HIDDEN REFRESH CYCLE



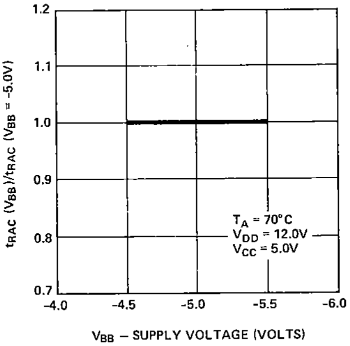
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{\text{CAS}}$ OR $\overline{\text{WE}}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{\text{CAS}}$ OR $\overline{\text{RAS}}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{\text{RAS}}$/$\overline{\text{CAS}}$ CYCLES PRECEEDED BY A $\overline{\text{CAS}}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{\text{CAS}}$ HAS NOT BEEN DECODED WITH $\overline{\text{RAS}}$).

TYPICAL CHARACTERISTICS[1]

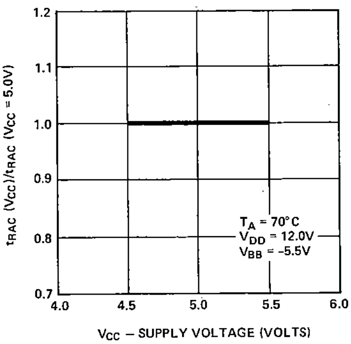
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{DD}



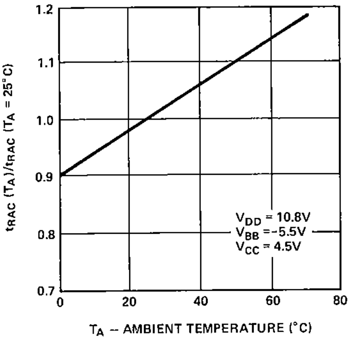
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{BB}



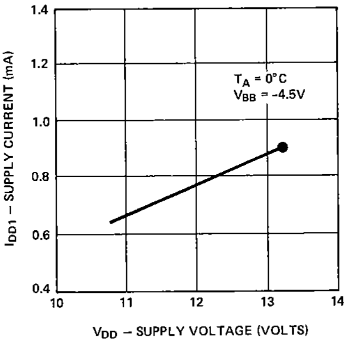
GRAPH 3
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{CC}



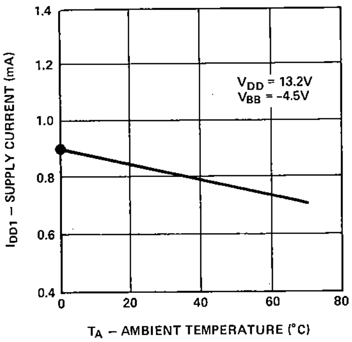
GRAPH 4
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS.
AMBIENT TEMPERATURE



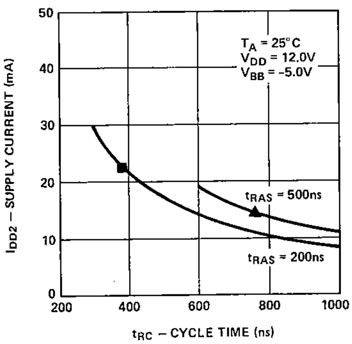
GRAPH 5
TYPICAL STANDBY CURRENT
I_{DD1} VS. V_{DD}



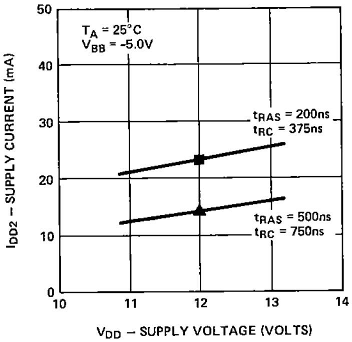
GRAPH 6
TYPICAL STANDBY CURRENT
I_{DD1} VS. AMBIENT TEMPERATURE



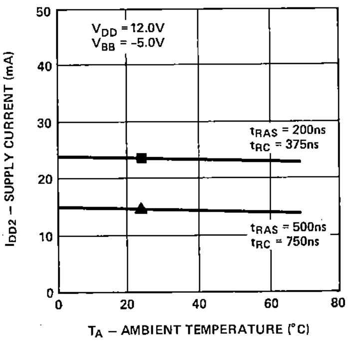
GRAPH 7
TYPICAL OPERATING CURRENT
I_{DD2} VS. t_{RC}



GRAPH 8
TYPICAL OPERATING CURRENT
I_{DD2} VS. V_{DD}



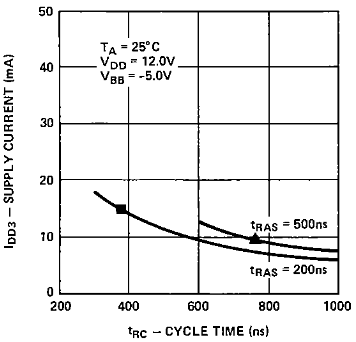
GRAPH 9
TYPICAL OPERATING CURRENT
I_{DD2} VS. AMBIENT TEMPERATURE



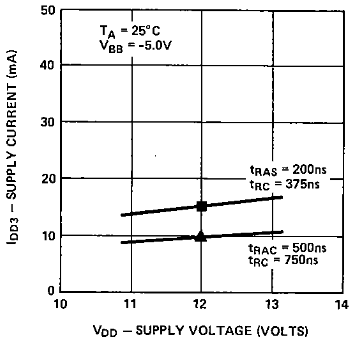
NOTES: See following page for Typical Characteristics Notes.

TYPICAL CHARACTERISTICS [1]

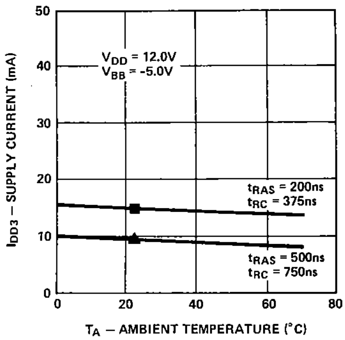
GRAPH 10
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. t_{RC}



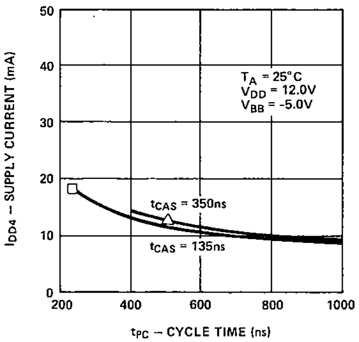
GRAPH 11
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. V_{DD}



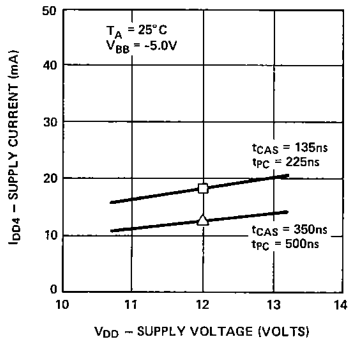
GRAPH 12
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. AMBIENT TEMPERATURE



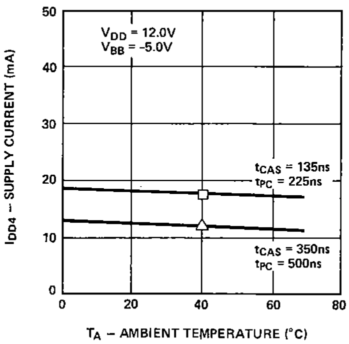
GRAPH 13
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. t_{PC}



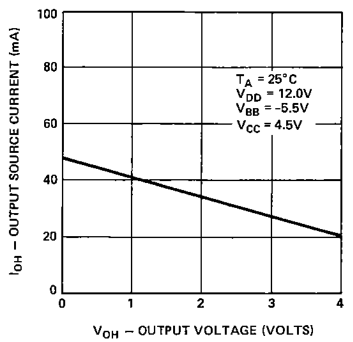
GRAPH 14
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. V_{DD}



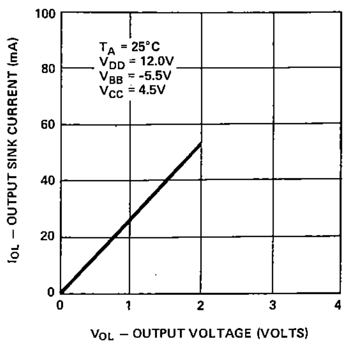
GRAPH 15
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. AMBIENT TEMPERATURE



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. OUTPUT VOLTAGE V_{OH}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. OUTPUT VOLTAGE V_{OL}



NOTES:

1. The cycle time, V_{DD} supply voltage, and ambient temperature dependence of I_{DD1}, I_{DD2}, I_{DD3} and I_{DD4} is shown in related graphs. Common points of related curves are indicated:
   - ● I_{DD1} @ V_{DD} = 13.2V, T_A = 0°C
   - ■ I_{DD2} or I_{DD3} @ t_{RAS} = 200ns, t_{RC} = 375ns, V_{DD} = 12.0V, T_A = 25°C
   - ▲ I_{DD2} or I_{DD3} @ t_{RAS} = 500ns, t_{RC} = 750ns, V_{DD} = 12.0V, T_A = 25°C
   - □ I_{DD4} @ t_{CAS} = 135ns, t_{PC} = 225ns, V_{DD} = 12.0V, T_A = 25°C
   - △ I_{DD4} @ t_{CAS} = 350ns, t_{PC} = 500ns, V_{DD} = 12.0V, T_A = 25°C

   The typical I_{DD} current for a given combination of cycle time, V_{DD} supply voltage and ambient temperature may be determined by combining the effects of the appropriate family of curves.

RAM

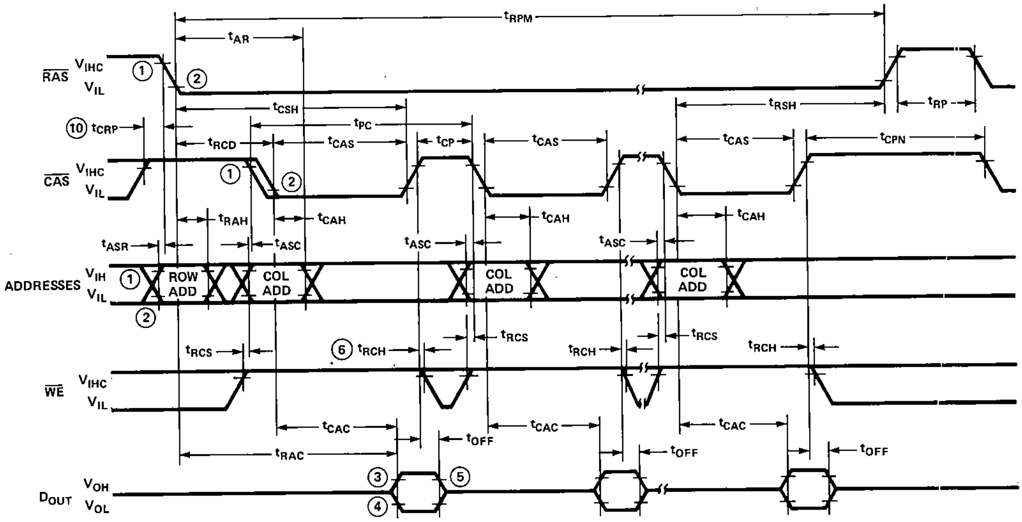
D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7,8,11]

T_A = 0°C to 70°C, V_{DD} = 12V±10%, V_{CC} = 5V±10%, V_{BB} = -5V±10%, V_{SS} = 0V, unless otherwise noted.
For Page Mode Operation order 2117-2 S6053, 2117-3 S6054, or 2117-4 S6055.

Symbol	Parameter	2117-2 S6053		2117-3 S6054		2117-4 S6055		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PC}	Page Mode Read or Write Cycle	170		225		275		ns	
t_{PCM}	Page Mode Read Modify Write	205		270		340		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	60		80		100		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	150	10,000	200	10,000	250	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		38		30		26	mA	9

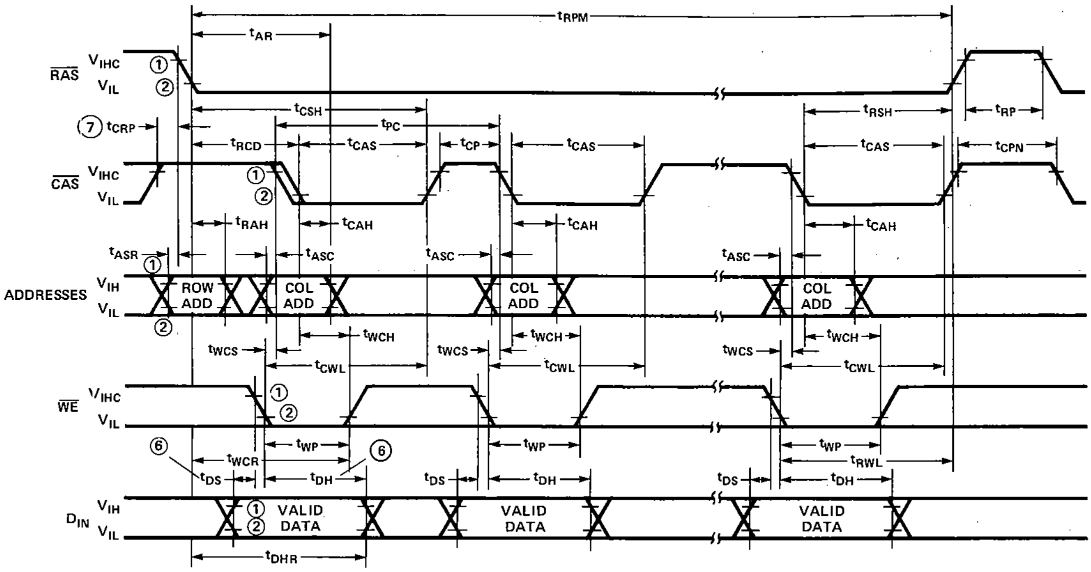
WAVEFORMS

PAGE MODE READ CYCLE

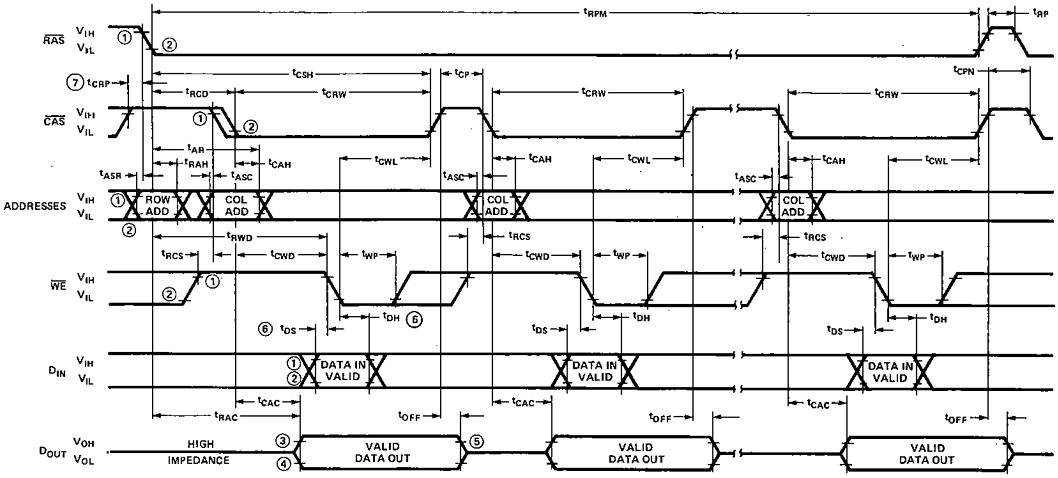


NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
7. ALL VOLTAGES REFERENCED TO V_{SS}.
8. AC CHARACTERISTIC ASSUME t_T = 5ns.
9. SEE THE TYPICAL CHARACTERISTICS SECTION FOR VALUES OF THIS PARAMETER UNDER ALTERNATE CONDITIONS.
10. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}/\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).
11. ALL PREVIOUSLY SPECIFIED A.C. AND D.C. CHARACTERISTICS ARE APPLICABLE TO THEIR RESPECTIVE PAGE MODE DEVICE (i.e., 2117-3, S6054 WILL OPERATE AS A 2117-3).

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

APPLICATIONS

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Device access time, t_{ACC}, is the longer of the two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the 2117-3 yields:

3. $t_{ACC} = t_{RAC} = 200$nsec for 25nsec $\leq t_{RCL} \leq 65$ nsec

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 135$ for $t_{RCD} > 65$nsec

Note that if 25nsec $\leq t_{RCD} \leq$65nsec device access time is determined by equation 3 and is equal to t_{RAC}. If t_{RCL} >65nsec, access time is determined by equation 4. This 40nsec interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 128 rows of the 2117 must be refreshed every 2 milliseconds to maintain data. Any memory cycle:

1. Read Cycle
2. Write Cycle (Early Write, Delayed Write or Read-Modify-Write)
3. $\overline{RAS}$-only Cycle

refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

DATA OUTPUT OPERATION

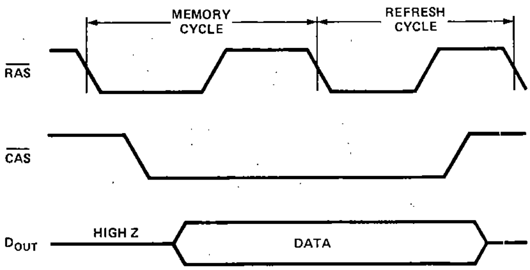
The 2117 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel 2117 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Fast Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the 2117 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

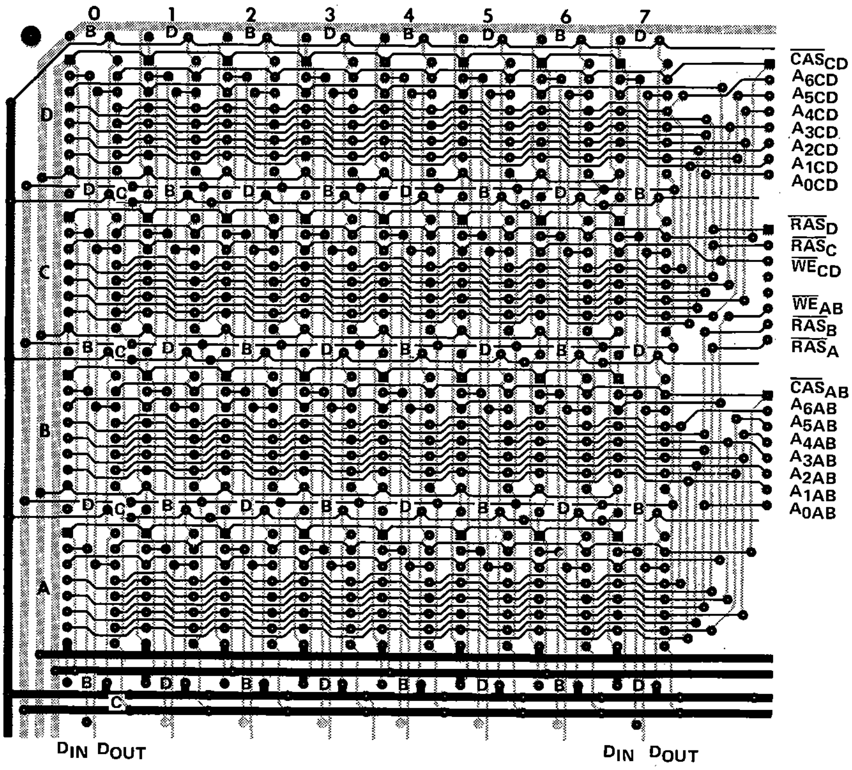
The 2117 requires no power on sequence providing absolute maximum ratings are not exceeded. After the application of supply voltages or after extended periods of bias (greater than 2 milliseconds) without clocks, the device must perform a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-Only refresh) prior to normal operation.

POWER SUPPLY DECOUPLING/DISTRIBUTION

It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

The V_{CC} supply is connected only to the 2117 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is associated with the input high level current to a TTL gate and the output leakage currents of any OR-tied 2117's (typically 100μA or less total). Intel recommends that a 0.1 or 0.01μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight memory devices.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1μF TO V_{DD} TO V_{SS}
B = 0.1μF V_{BB} TO V_{SS}
C = 0.01μF V_{CC} TO V_{SS}

SAMPLE P.C. BOARD LAYOUT EMPLOYING VERTICAL AND HORIZONTAL GRIDDING ON ALL POWER SUPPLIES.

BOARD ORGANIZATION: 64K WORDS BY 8-BITS.

64K BYTE STORAGE ARRAY LAYOUT